

ARC[®] 625D CONFIGURABLE CORE

PROCESSOR

Configurable, General Purpose 32-Bit CPU/DSP
Core for Cost-Sensitive Applications

Applications

CONSUMER PRODUCTS

- Low cost set-top boxes
- Personal audio and image players
- Cellular handsets

NETWORK DEVICES

- Broadband modems
- Wireless LANs
- VoIP terminals and gateways
- Home gateways

AUTOMOTIVE CONTROL

- Chassis and body systems

IMAGING

- Inkjet printers
- Multi-function peripherals

INDUSTRIAL CONTROL

The ARC[®] 625D processor core is a full-featured, mid-range embedded core with best-in-class speed, die area and power characteristics. It is designed as a complete processor solution for SoCs targeted at consumer, networking, automotive and other cost-sensitive markets.

The ARC 625D core's flexible, configurable memory architecture makes it ideal for RTOS-based applications. Powerful DSP options enable it to perform more functions, eliminating separate logic or DSP blocks from the SoC. Optionally, custom instruction extensions may be incorporated to achieve application performance levels unattainable with fixed architecture cores.

Product characteristics in 90nm process*

Max Clock Frequency	500 MHz
Power Consumption	0.05 mW/MHz
Silicon Area	0.25 mm ²

*Frequency (worst case condition) is based on TSMC GT. Power (typical condition) and area are based on TSMC LP process. Data is for base configuration, placed and routed design excluding RAMs.

Highlights

- A highly configurable architecture allows SoC designers to include only the processor features that are required for their specific application, resulting in smaller die size and lower power than can be achieved with a fixed core.
- User-defined instruction and register extensions deliver 5 – 100 times performance improvement of critical routines.
- Flexible memory design including caches and closely coupled (single-cycle) memories is ideal for RTOS-based applications.
- Built-in DSP features include instruction and register extensions that accelerate signal processing algorithms.
- Optional ARC XY Advanced DSP subsystem delivers the performance of dedicated DSP cores.
- ARCompact™ 16-/32-bit Instruction Set Architecture reduces code size by up to 40 percent compared to 32-bit only instruction sets.
- JTAG debug port and optional embedded hardware breakpoints facilitate software debug.
- Delivered as synthesizable RTL source code (Verilog[®]), the ARC 625D core is fully compatible with industry standard design methodologies and tool flows.



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ARC® 625D Core Features

CPU Architecture

- 5-stage instruction pipeline
- Static branch prediction
- 32-bit data, instruction and address buses
- Scoreboarded data memory pipeline to reduce data stalls
- Single-cycle instruction CCM (Closely Coupled Memory), 1KB – 512KB
- Single-cycle data CCM, 2KB – 256KB
- Configurable instruction cache, 2KB – 32KB
- Configurable data cache, 2KB – 32KB
- Configurable endianness
- Up to 32, two level interrupts

ARCompact™ ISA

- 16- and 32-bit instructions for high code density
- No overhead for switching between 16- and 32-bit
- Single-cycle instruction execution
- Up to 128 dual or single operand instruction codes available for user-defined extensions
- Up to 64 directly addressable core registers and 32 conditional execution codes
- Flexible addressing modes

Registers

- 16 or 32 entry register file in base processor, extendible to 60
- 32-bit auxiliary register space for single-cycle, unarbitrated data storage and retrieval

DSP Extensions

- 16- and 32-bit MUL and MAC instructions
- Parallel execution of MUL, MAC and other ALU operations
- Saturating arithmetic instructions
- Zero overhead loop support

ARC XY Advanced DSP Subsystem

- For more information, see ARC XY Subsystem product brief

Power Management

- Sleep mode via software instruction
- Clock gating option
- High efficiency pipeline
- On-chip RAM controls

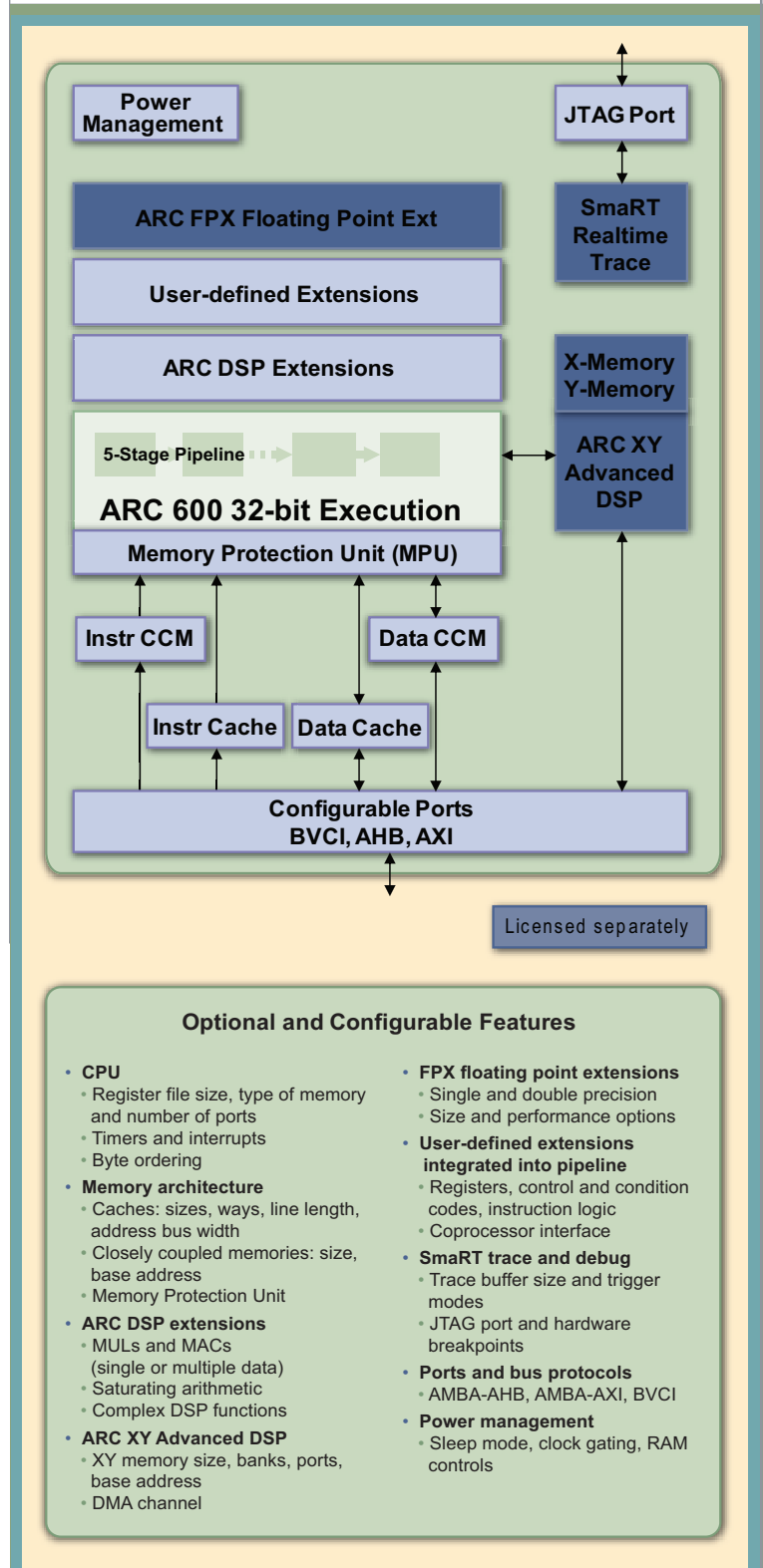
Host Interface/Debug Features

- Software and hardware breakpoints with cascadable triggers
- JTAG interface to host tools
- Debug host can access all registers and CPU memory
- Supported by leading debuggers including Green Hills Software and MetaWare™

System Interface

- Configurable port complies with industry standard AMBA or BVCI
- Slave interfaces exposed for loading optional instruction and data CCMs

ARC® 625D CORE



Optional and Configurable Features

- **CPU**
 - Register file size, type of memory and number of ports
 - Timers and interrupts
 - Byte ordering
- **Memory architecture**
 - Caches: sizes, ways, line length, address bus width
 - Closely coupled memories: size, base address
 - Memory Protection Unit
- **ARC DSP extensions**
 - MULs and MACs (single or multiple data)
 - Saturating arithmetic
 - Complex DSP functions
- **ARC XY Advanced DSP**
 - XY memory size, banks, ports, base address
 - DMA channel
- **FPX floating point extensions**
 - Single and double precision
 - Size and performance options
- **User-defined extensions integrated into pipeline**
 - Registers, control and condition codes, instruction logic
 - Coprocessor interface
- **SmaRT trace and debug**
 - Trace buffer size and trigger modes
 - JTAG port and hardware breakpoints
- **Ports and bus protocols**
 - AMBA-AHB, AMBA-AXI, BVCI
- **Power management**
 - Sleep mode, clock gating, RAM controls

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For more information on ARC's products and services visit our corporate website at: www.ARC.com.

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