

ARC™ XY ADVANCED DSP

Applications

BASEBAND PROCESSING

- 2G and 3G cellular handsets
- xDSL home gateway
- Cordless phone
- COFDM

MULTI-MEDIA CODECS

- Audio decoding and encoding
- Video decoding and encoding
- Still image manipulation

STORAGE APPLICATIONS

- Hard drive control

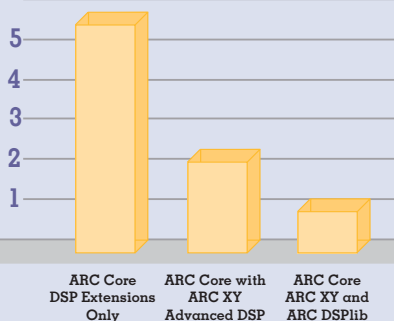
VOICE

- Cellular voice codec
- Voice over IP codecs
- Voice recognition

SECURITY

- Encryption acceleration
- Image recognition
- Fingerprint identification
- DRM acceleration

Normalized Performance for 256 point FFT (Number of CPU cycles)



Full Performance Digital Signal Processing for ARC Configurable Cores

ARC™ XY Advanced DSP adds the power of a true DSP engine to ARC CPU cores, enabling conventional and signal processing computation within a single unified architecture. ARC XY Advanced DSP may be applied to most of the cores within the ARC 600 and ARC 700 families.

ARC also offers DSPlib, a library of frequently used signal processing functions that have been verified and optimized for ARC XY Advanced DSP. The library takes full advantage of ARC's extendible instruction architecture to maximize the performance of each function.

ARC cores with ARC XY Advanced DSP provide a complete solution for many complex computation problems in SoCs that are targeted at communications, media processing and many other applications.

Highlights

Accelerate data processing: ARC XY Advanced DSP's separate memory banks for X and Y operands deliver data at register speed, eliminating main memory fetch cycles. In addition, ARC XY Advanced DSP's address generators eliminate the CPU cycles to determine the address of the performance of a dedicated DSP engine.

Eliminate separate DSP and logic blocks: Many applications use a CPU core for control functions and a separate DSP core or dedicated hardware for codec and other data stream processing functions. An ARC core with ARC XY Advanced DSP can replace separate DSP hardware and its associated memory with an efficient, single-processor solution.

Consolidate development environment: Developers who code for separate CPU and DSP architectures must purchase, learn, and maintain two sets of development tools. An ARC core with ARC XY Advanced DSP (or one ARC core configured for control processing and a second configured for DSP) requires only a single unified environment.

XY Memory Architecture

The ARC XY Advanced DSP architecture is built around two memory structures, X and Y, which source two operands and receive results in the same cycle.

Data in the XY memory is indexed via pointers from address generators and supplied to the ARC CPU pipeline for processing by any ARC instruction. The memories are software-programmable to provide 32-bit, 16-bit, or dual 16-bit data to the pipeline.

Additionally, an internal DMA engine moves data in and out of XY memory without impacting the processor pipeline.

Memory Configuration Options

| ARC XY with 600 family core | ARC XY with 700 family core |
|-----------------------------|-----------------------------|
| Single or dual port | Dual port |
| 1 or 2 banks | 1 bank |
| 1KB – 32KB per bank | 8KB – 64KB |

Address Generator Facilities

The ARC XY Advanced DSP address generators make complex address calculations independently, removing a significant overhead from the CPU.

The address generators operate in several addressing modes under software control to optimize performance on DSP algorithms:

- Variable offset
- Modulo
- Bit reverse

The address may either be updated after access or remain unchanged depending on the instruction.

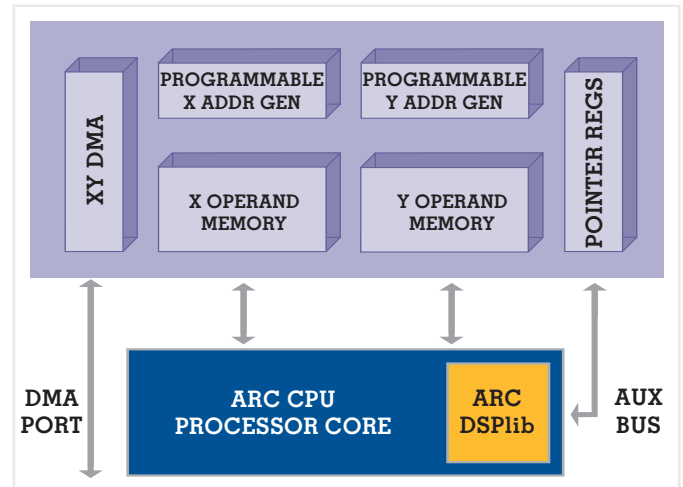
ARC™ DSPlib

ARC DSPlib is a library of instruction extensions developed and verified by ARC to accelerate common DSP processing algorithms. This library allows any of these instructions to be applied to an ARC core with ARC XY Advanced DSP by a simple drag and drop in the ARChitect™ Processor Configurator tool.

Example ARC DSPlib extensions include:

- Dual FFT
- Viterbi
- CRC
- 24 x 24 MAC

ARC™ XY ADVANCED DSP



Licensed separately

Design Example

The first design of a cordless phone SoC for a high volume manufacturer included a 32-bit CPU core and a separate DSP. Competitive pressure forced a cost reduction respin. They turned to ARC's CPU/DSP core with ARC XY Advanced DSP.

The result was elimination of over 150,000 gates, reduced memory requirements, reduced power, a single tool chain for software development, and a successful project.



NORTH AMERICA:

ARC International
2025 Gateway Place, Suite 140
San Jose, CA 95110
Tel: +1 408 437 3400
Fax: +1 408 437 3401

EUROPE:

ARC International
The Waterfront, Elstree Road
Elstree, Herts. WD6 3BS UK
Tel: +44 (0) 20 8236 2800
Fax: +44 (0) 20 8236 2801

ASIA:

ARC International Japan
Tel: +81 (3) 5532 7250
ARC International Taiwan
Tel: +886 2 2657 7824



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