

ARC[®] 610D CORE

PROCESSOR

Small, Low Power Embedded Core Combines
32-Bit CPU and Powerful DSP Features

Applications

PORTABLE CONSUMER PRODUCTS

- Personal audio and image players
- Digital still cameras
- Entry level cellular handsets
- Handheld games and toys

AUTOMOTIVE CONTROL

- Chassis and body systems

MASS STORAGE PRODUCTS

- Disk drives
- DVD players

MULTI-CORE DESIGNS FOR NETWORK APPLICATIONS

The ARC[®] 610D core processor core is ideal for SoC applications which include conventional computation and signal processing algorithms. The core is designed for hard, real-time processing, where high speed and deterministic response are required.

Powerful and flexible DSP options enable the 610D to perform more functions, eliminating separate logic or DSP blocks from the SoC. Optionally, custom instruction extensions may be incorporated, to achieve application performance levels unattainable with fixed architecture cores.

Product characteristics in 0.13 μ m process*

Max Clock Frequency	260 MHz
Power Consumption	0.07 mW/MHz
Silicon Area	0.64 mm ²

*Worst case results for base configuration, excluding memory

Highlights

- A highly configurable architecture allows SoC designers to include only the processor features which are required for their specific application, resulting in smaller die size and lower power than can be achieved with a fixed core.
- User-defined instruction and register extensions deliver 5 – 100 times performance improvement of critical routines.
- Cacheless design and closely coupled (single-cycle) memories provide fast, predictable computation.
- Built-in DSP features include instruction and register extensions that accelerate signal processing algorithms.
- Optional ARC XY Advanced DSP subsystem delivers the performance of dedicated DSP cores.
- ARCCompact™ 16-/32-bit Instruction Set Architecture reduces code size by up to 40 percent compared to 32-bit only instruction sets.
- JTAG debug port and optional embedded hardware breakpoints facilitate software debug.
- Delivered as synthesizable RTL source code (Verilog[®]), the ARC 610D core is fully compatible with industry standard design methodologies and tool flows.



ARC® 610D Features

CPU Architecture

- 5-stage instruction pipeline
- Static branch prediction
- 32-bit data, instruction and address buses
- Scoreboarded data memory pipeline to reduce data stalls
- Single-cycle instruction CCM (Closely Coupled Memory), 1KB – 512KB
- Single-cycle data CCM, 2KB – 16KB
- Configurable endianness
- Up to 32, two level interrupts

ARCompact™ ISA

- 16- and 32-bit instructions for high code density
- No overhead for switching between 16- and 32-bit
- Single-cycle instruction execution
- Up to 128 dual or single operand instruction codes available for user-defined extensions
- Up to 64 directly addressable core registers and 32 conditional execution codes
- Flexible addressing modes

Registers

- 16 or 32 entry register file in base processor, extendible to 60
- 26 general purpose registers, extendible to 54
- 32-bit auxiliary register space for single-cycle, unarbitrated data storage and retrieval

DSP Extensions

- 16- and 32-bit MUL and MAC instructions
- Dedicated registers enable parallel execution of MUL, MAC and other ALU operations
- Saturating arithmetic instructions
- Zero overhead loop support

AR XY Advanced DSP Subsystem

- For more information, see ARC XY Subsystem product brief

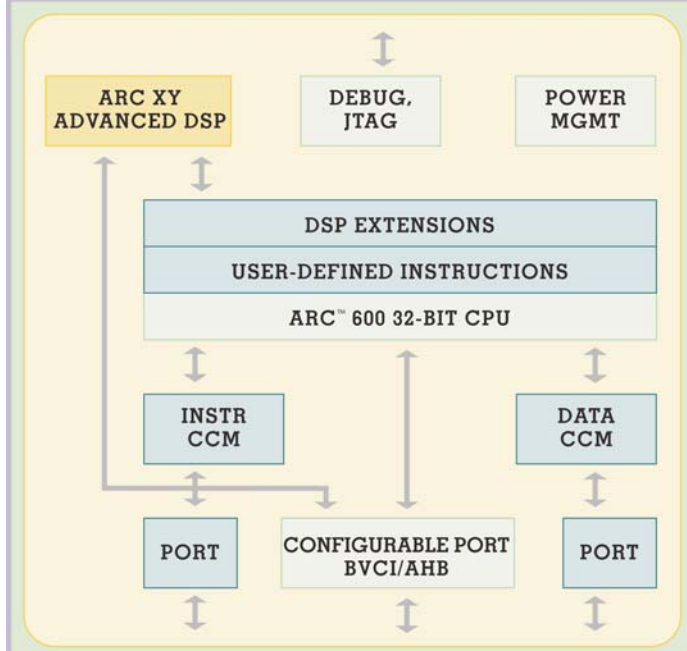
Power Management

- Sleep mode via software instruction
- Clock gating option
- High efficiency pipeline
- On-chip RAM controls

Host Interface/Debug Features

- Software and hardware breakpoints with cascadable triggers
- JTAG interface to host tools
- Debug host can access all registers and CPU memory
- Supported by leading debuggers including Green Hills Software and MetaWare®

ARC® 610D CORE



KEY: **ARC XY LICENSED SEPARATELY** **OPTIONAL**



System Interface

- Configurable port complies with industry standard AMBA or BVC1
- Slave interfaces exposed for loading optional instruction and data CCMs

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