

# ARC<sup>®</sup> 605 CONFIGURABLE CORE

PROCESSOR

World's Smallest, Lowest Power and  
Most Configurable 32-Bit CPU Core

## Applications

### PORTABLE CONSUMER PRODUCTS

- Digital still cameras
- Cordless phones
- Handheld games and toys

### AUTOMOTIVE CONTROL

- Chassis and body systems

### MASS STORAGE PRODUCTS

- Disk drives
- DVD players

### MULTI-CORE DESIGNS FOR NETWORK APPLICATIONS

- Packet processing
- Security accelerators
- TCP offload engines

### 8- AND 16-BIT MICROCONTROLLER DESIGN UPGRADES

### DEEPLY EMBEDDED PROGRAMMABLE STATE MACHINES

The ARC<sup>®</sup> 605 processor core is an ideal solution for a wide range of embedded control and computing functions within SoCs. The core is designed for hard real-time processing, where high speed and deterministic response are required.

The highly configurable ARC 605 core is smaller, lower power and provides up to twice the MHz performance of competing cores. Optionally, custom instruction extensions may be incorporated to achieve application performance levels unattainable with fixed architecture cores.

## Highlights

- A highly configurable architecture allows SoC designers to include only the processor features that are required for their specific application, resulting in smaller die size and lower power than can be achieved with a fixed core.
- User-defined instruction and register extensions deliver 5 – 100 times performance improvement of critical routines.
- Cacheless design and closely coupled (single-cycle) memories provide fast, predictable computation.
- ARCompact™ 16-/32-bit Instruction Set Architecture reduces code size by up to 40 percent compared to 32-bit-only instruction sets.
- JTAG debug port and optional embedded hardware breakpoints facilitate software debug.
- Delivered as synthesizable RTL source code (Verilog<sup>®</sup>), the ARC 605 core is fully compatible with industry standard design methodologies and tool flows.

## Product characteristics in 0.13µm process\*

Max Clock Frequency	250 MHz
Power Consumption	0.06 mW/MHz
Silicon Area	0.31 mm <sup>2</sup>

\*Worst case results for base configuration, excluding memory



# ARC® 605 Core Features

## CPU Architecture

- 5-stage instruction pipeline
- Static branch prediction
- 32-bit data, instruction and address buses
- Scoreboarded data memory pipeline to reduce data stalls
- Single-cycle instruction CCM (Closely Coupled Memory), 1KB – 512KB
- Single-cycle data CCM, 2KB – 16KB
- Configurable endianness
- Up to 32, two-level interrupts

## ARCompact™ ISA

- 16- and 32-bit instructions for high code density
- No overhead for switching between 16- and 32-bit
- Single-cycle instruction execution
- Up to 128 dual or single operand instruction codes available for user-defined extensions
- Up to 64 directly addressable core registers and 32 conditional execution codes
- Flexible addressing modes

## Registers

- 16 or 32 entry register file in base processor, extendible to 60
- 26 general purpose registers, extendible to 54
- 32-bit auxiliary register-space for single-cycle, unarbitrated data storage and retrieval

## Power Management

- Sleep mode via software instruction
- Clock gating option
- High-efficiency pipeline
- On-chip RAM controls

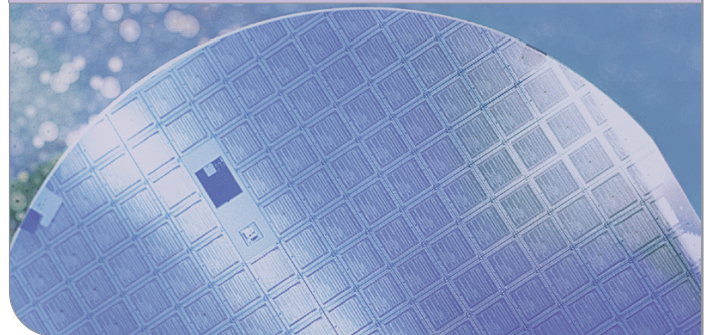
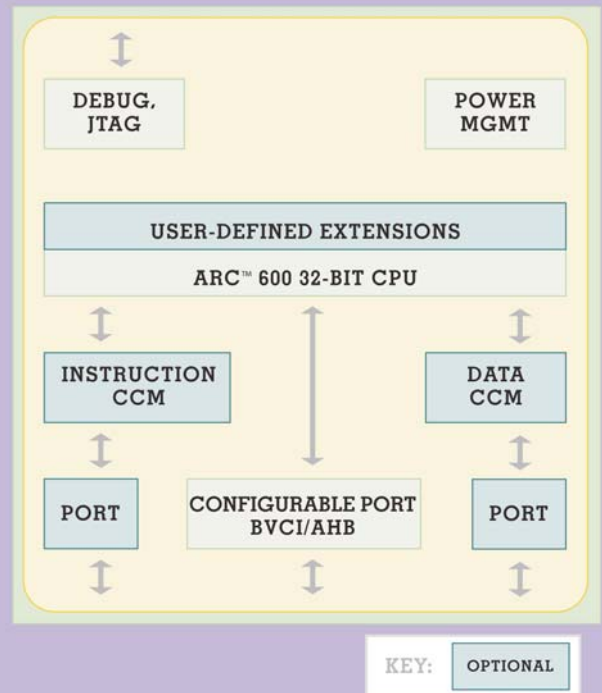
## Host Interface/Debug Features

- Software and hardware breakpoints with cascadable triggers
- JTAG interface to host tools
- Debug host can access all registers and CPU memory
- Supported by leading debuggers, including Green Hills Software and MetaWare®

## System Interface

- Configurable port complies with industry-standard AMBA or BVCI
- Slave interfaces exposed for loading optional instruction and data CCMs

# ARC® 605 CORE



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