

# ARC<sup>®</sup> 600 CONFIGURABLE CORE FAMILY

CORE FAMILY

## Applications

### CONSUMER PRODUCTS

- Low cost set-top boxes
- Personal audio and image players
- Digital still cameras
- Cordless phones
- Entry level cellular handsets
- Handheld games and toys

### NETWORK DEVICES

- Broadband modems
- Wireless LANs
- VoIP terminals and gateways
- Home gateways

### AUTOMOTIVE CONTROL

- Chassis and body systems

### MASS STORAGE PRODUCTS

- Disk drives
- DVD players

### IMAGING

- Inkjet printers
- Multi-function peripherals

### MULTI-CORE DESIGNS FOR NETWORKING APPLICATIONS

- Storage area networks
- Packet processing
- Security accelerators
- TCP offload engines

### INDUSTRIAL CONTROL

### 8- AND 16-BIT MICROCONTROLLER DESIGN UPGRADES

### DEEPLY EMBEDDED STATE MACHINES

## Best-in-Class, 32-Bit CPU/DSP Cores for Embedded SoC Processing

The ARC<sup>®</sup> 600 family of configurable cores is designed for embedded control, computation and DSP tasks in SoCs for consumer, networking, automotive and many other markets.

The core family is ideal for battery-operated and cost-sensitive products.

### Lean:

The configurable architecture of the ARC 600 family allows SoC designers to select only the processor features that are required for their specific application, achieving smaller die size and lower power than is possible with a fixed core.

### Efficient:

SoC designers can optimize application efficiency by defining extensions to the ARC 600 architecture, providing higher application performance than can be achieved with a fixed core. Alternatively, frequency can be lowered, resulting in a lower power core.

### Hard Working:

The ARC 600 family's powerful DSP options allow the SoC designer to implement more functionality in the processor core and eliminate external logic or DSP blocks.

	ARC 605	ARC 610D	ARC 625D
Type of Processing	Hard, Real-Time Embedded	General Purpose Embedded	Applications, Open OS
ARC <sup>®</sup> 600 execution unit	Yes	Yes	Yes
User-defined extensions	Optional	Optional	Optional
DSP extensions	No	Optional	Optional
ARC XY Advanced DSP	No	Optional	Optional
Closely coupled memory <sup>1</sup>	1-512KB/2-16KB	1-512KB/2-16KB	1-512KB/2-16KB
Cache <sup>1</sup>	No	No	0 32KB/0 32KB
Max. Clock frequency <sup>2</sup>	400 MHz	400 MHz	350 MHz
Power consumption <sup>2</sup>	0.06 mW/MHz	0.07 mW/MHz	0.08 mW/MHz
Silicon area <sup>2</sup>	0.31 mm <sup>2</sup>	0.64 mm <sup>2</sup>	0.71 mm <sup>2</sup>

1. Instruction/Data 2. Worst case results in a typical 0.13µm process for base configuration excluding memory



# ARC<sup>®</sup> 600 Architecture

## CPU Architecture

The ARC 600 32-bit architecture employs a highly efficient 5-stage pipeline, achieving 1.3 DMIPS/MHz.

The architecture includes flexible memory options to address a wide range of processing needs. These include single-cycle Closely Coupled Memories (CCMs) for instructions and data, as well as configurable I-cache and D-cache.

External access is via multiple 32-bit ports, including main memory, auxiliary registers and CCMs. BVCI and AHB configuration options are supported.

## ARCompact™ ISA

Up to 40 percent improvement in code density can be achieved with the ARCompact 16-/32-bit ISA. 16- and 32-bit instructions are freely mixed by compilers without overhead.

## Powerful DSP Features

The ARC 600 family provides true DSP on a RISC pipeline, with performance up to 500 MMACs per second in a 0.13µm process.

- ARC 600 DSP Extensions include 16- and 32-bit MAC and saturating arithmetic instructions
- ARC XY Advanced DSP provides full DSP performance by adding configurable banks of XY memory
- ARC DSPlib is a library of custom instructions to greatly accelerate common DSP calculations

## Software Development

ARC 600 cores are supported by the industry's leading development environments including optimized compilers:

- ARC MetaWare<sup>®</sup> Suite
- Green Hills Software Multi Suite
- GNU

Modeling tools are available to accelerate time to market through parallel software and hardware development:

- Functional Instruction Set Simulator ensures functionality of the code with execution speeds approaching hardware
- Cycle Accurate Model provides additional timing information for core operation
- MetaSim™ co-simulation suite allows the ISS to work with HDL simulation
- ARCangel™ FPGA emulation board provides fast emulation capability



## Highly Configurable

ARC enables designers to add features they need and remove features they do not need for their individual application. The menu of options includes type and size of caches, interrupts, DSP features, timers, etc. Performance, size and power tradeoffs are quickly accomplished and the resulting optimized solution will invariably have smaller area and lower production cost than a fixed processor core.

Custom configurations are created using the drag and drop GUI of ARC's ARChitect™ Processor Configurator tool.

## User-Defined Extensions

ARC offers the flexibility to add instructions, registers, flags and condition codes, creating a processor that is highly tuned for the specific application. Reduction of up to 100 times in the number of clock cycles required for inner loops or repetitive software can be achieved with the intelligent use of user-defined instructions. The result is higher application performance and/or lower device frequency and lower power than is possible with a fixed instruction set.

Extensions are created directly in SystemC or Verilog<sup>®</sup> using ARC's Extension Instruction Automation tool suite and templates.

## On-chip Debug Features

Each core's JTAG interface allows a debug host to set software breakpoints, examine or change memory and register values, and step through the target code. Optional hardware breakpoints can be added.

## RTOS and Application Software

The ARC 600 family is supported by a large third party development community. Available industry standard software ports include:

- ThreadX
- MQX
- Java
- µltron
- µCLinux

Applications for audio, video, VoIP, networking, USB, and others are also available from third party developers or ARC.

### NORTH AMERICA:

ARC International  
3590 N. First Street, Suite 200  
San Jose, CA 95134  
Tel: +1 408 437 3400  
Fax: +1 408 437 3401

### EUROPE:

ARC International  
Verulam Point, Station Way  
St Albans AL1 5HE UK  
Tel: +44 (0) 1727 89 1400  
Fax: +44 (0) 1727 89 1401

### ASIA:

ARC International Greater China  
Tel: +886 (3) 5788198  
  
ARC International Japan  
Tel: +81 (3) 5847 7950



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